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No fee is required for the present amendment. The number of claims remains the same as the number originally filed. Dependent claim 27 has been cancelled, and a new dependent claim 31 has been added.

New claim 31 covers batch cleaning processes described on pages 20-23, 45-47 and 69 of the specification wherein 10 to 20 semiconductor wafers are cleaned simultaneously while the front face of each wafer is charged to promote removal of contaminant sub 0.05-micron particles. The wafer cleaning operations at existing fabrication plants can, of course, utilize 5-tank or 7-tank wet benches of the type described on page 21 of the specification, for example, with or without the assistance of megasonic transducer means.

It is noted that claims 9 to 13 have been allowed and that apparatus claims 15 to 17 have been withdrawn from consideration. The remaining claims 1-8, 14 and 18-30 have been rejected.

The Examiner's objection to the language of claim 13 is not understood and is believed to be unwarranted because the meaning of the claim is clear and definite. It is not seen how any amendment could clarify or improve the claim.

Claims 1, 2, 4, 8, 18, 21, 26 and 28 have been rejected under 35 USC 102(e) as being anticipated by Flitsch Patent No. 6,136,669 which relates to the prevention of ionic contamination by alkali mobile ions that can adversely affect silicon device reliability. The Examiner perhaps has some basis for believing

or contending that ions are smaller than 0.1 micron particles and that the water rinse described in the Flitsch patent might be preceded by a CMP operation. However, his description of the Flitsch method otherwise seems to be inaccurate or incorrect because that patent clearly does not anticipate the process claimed by applicant. It appears that the process described in that patent cannot satisfy or meet the terms of any of the claims now presented in this case. The rejections based on that patent are questionable and would seem to be unwarranted. Reconsideration of the rejection is requested.

Attention is directed to the fact that applicant's wafer cleaning process is quite different from that of the Flitsch patent because of substantially different operating temperature. Applicant's process can perhaps be carried out at temperatures sometimes as high as 100°C (See page 16, line 6), but the operating temperature usually would be less or in a range no higher than that disclosed on page 11 (e.g., 70° to 85°C) and more likely closer to 70°C (See pages 17 and 18).

It is believed that the Flitsch patent is not particularly pertinent with respect to applicant's patent claims because it discloses a higher temperature, such as 200°C or more as indicated in claim 4 of that patent and also in the sixth paragraph of the Detailed Description which reads "The wafer 112, represented by the device structure, is held on a wafer chuck 114, where it is subjected to bias-temperature conditions of 1 MV/cm at 200°C to 300°C for 2 to 3 minutes."

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The "Experimental Results" described in the Flitsch specification states "After corona biasing, both wafers were uniformly heated to 200°C." The Flitsch patent includes a citation of a related U.S. Patent No. 5,701,088 (Fujimaki) that recommends a temperature in the range of 100° to 300°C. The simple fact is that the corona-discharge technique of the Flitsch patent usually involves operating temperatures higher than those preferred by applicant. That technique is not believed to be pertinent to applicant's claimed invention and does not appear to teach or suggest the wet cleaning process of the present invention wherein the operating temperature preferably does not exceed 85°C (e.g., as in an RCA-type wafer cleaning system wherein an excessive temperature might adversely affect the ammonium hydroxide or the hydrogen peroxide).

A brief review of Flitsch Patent No. 6,136,669 confirms that it discloses and claims a process wherein a corona discharge bias is applied to one face of a semiconductor wafer while heating the wafer to an elevated temperature above 100°C to cause mobile alkali ions to move out to the wafer surface. The wafer is at such an elevated temperature as the electric charge is applied to generate an electric field of 1 to 2 MV/cm.

The Flitsch patent does not disclose or suggest applicant's process for wet cleaning of semiconductor wafers (e.g., as defined in claim 7, 21, 22 or 26) wherein the wafer face is charged to provide a small but effective field intensity, such as 0.02 volt/mm or more, sufficient to remove and repel sub 0.1-micron particles. That patent apparently does not disclose a

process capable of removing such fine particles and does not seem to be pertinent to the invention as claimed herein. The patent does not teach use of a limited voltage, such as 2 to 60 volts, as claimed herein that is sufficient to cause efficient removal of harmful sub 0.05-micron particles. The water rinse of Flitsch obviously cannot function in that manner.

In rejecting claims 3, 7, 23-25, 27 and 30 under 35 USC 103(a), the Examiner contends that it would be obvious to modify the process disclosed by Flitsch and to employ a relatively low voltage of only 3 volts as taught by Kishii et al (JP406232103). However, there appears to be no teaching or compelling reason to combine these dissimilar patent references (in the absence of applicant's own disclosure).

The proposed combination of references is believed to be questionable and unwarranted for several reasons. First, the law would seem to require a secondary reference to be part of the "common knowledge" in the art rather than an obscure disclosure known to few persons skilled in the art. There appears to be (1) no "common knowledge" that could lead a person skilled in the art to reduce the voltage in the process of Flitsch and (2) nothing clearly suggesting that sub 0.05-micron "killer" particles (i.e., "killer defects") could be removed when employing a low voltage, such as 3 volts. It is not seen how, in the absence of hindsight, there is a logical or proper basis for the Examiner's contention that such voltage "would allow the removal of the desired impurities" even with the assistance of megasonic energy. A fourth reason is that the proposed combination of references

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fails to fully meet the terms of the claims (e.g., claims 5, 19, 25 and 28-30) which require charging of the wafers during chemical treatments (e.g., before rinsing).

In his rejection of dependent claims 5, 6, 19, 20 and 22, the Examiner refers to "admitted prior art" and particularly disclosures by applicant of common practice in the semiconductor industry (e.g., CMP and RCA clean processes). Such matters of common knowledge can properly be considered when determining the obviousness of proposed changes in the processes of the Flitsch patent, but all of the rejections based on that patent are believed to be questionable and unwarranted for the reasons set forth previously.

It is believed that applicant's invention as claimed herein has patentable merit and is not taught by the prior art. The specification indicates at page 45, for example, that a limited voltage of 2 to 60 volts insufficient to damage a modern advanced microchip (e.g., with a line width or feature size no more than 0.15 micron) can provide effective removal of "killer" particles in the sub 0.1-micron range (e.g., from 0.02 to 0.05 micron) which heretofore could not be removed satisfactorily by known methods.

The Examiner seems to believe or assume that a process of the type described in Flitsch Patent No. 6,136,669 could obtain a similar result using higher voltages as disclosed in that patent even though the patent describes a solution to a somewhat different problem caused by mobile ions. It is not

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seen how the description in that patent supports the Examiner's assumptions or the rejections of the claims.

It is believed that the rejected process claims of this application distinguish from the prior art and that the rejections under 35 USC 102 and 103 should be reconsidered and withdrawn. Allowance of the application is requested.

Respectfully submitted,

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